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GENERATION AND REGISTRATION OF DISTURBANCES IN A GAS FLOW.
1. FORMATION OF ARRAYS OF TUBULAR MICROHEATERS AND MICROSENSORS

V. A. Seleznev,[1] **V. Ya. Prinz,**[1] **V. M. Aniskin,**[2] **and A. A. Maslov**[2]

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A new method is proposed for creating "smart" surfaces for suppressing turbulence and retaining a laminar supersonic flow. Methods of formation of super-fast-response sensors and actuators for such surfaces are developed. Such sensors and actuators are structurally designed as microtubes made of $SiO_2/Si_3N_4/Au$ *and* InGaAs/GaAs/Au *heterofilms and suspended above a substrate; the wall thickness of these tubes is in the nanometer range; the tubes are connected to electrical contacts. Models of distributed arrays of tubular microsensors and microactuators are fabricated in a single technological process, which involves the well-established planar technology and the technology of rolling of stressed heterofilms.*

Key words: *tubular sensors and actuators, arrays of microtubes, flow control.*

Solving the problem of suppressing turbulence and retaining the laminar flow past the surface of new flying vehicles will substantially reduce the drag force, make the vehicle more cost-efficient, and improve its maneuvering and aerodynamic characteristics. For a subsonic flow, this problem can be solved with the use of microelectromechanical systems [1, 2]. For a supersonic flow, however, it is necessary to use fast-response microsensors and microactuators operating at frequencies above 1 MHz, which cannot be ensured by mechanical devices.

The present paper describes the technologies of formation of fast-response microsensors and microheaters (microactuators) and their design. The basis for such devices is the electroconducting microtubes with nanometer-thick walls. The advantage of thin-walled tubular elements is a short time of their thermal relaxation $\tau \approx 1$ μsec [3, 4], which is significantly smaller than the time of thermal relaxation of standard wire ($\tau \approx 1$ msec) or film elements. Fast-response local tubular microheaters and microsensors forming regular controlled arrays on the flying vehicle surface are designed to assist in formation of "smart" surfaces improving the aerodynamic characteristics of flying vehicles, first of all, small-scale vehicles.

Methods developed to form tubular microsensors, microheaters-actuators, and their arrays (systems) are described below. Such methods are widely used and seem to be promising in fabrication of "smart" surfaces with rather large areas.

In the system proposed, the tubular elements used as microactuators are identical to microsensors (Fig. 1). Using an additional integrated processor, one can rapidly switch a necessary tube between the sensor and actuator modes, thus, changing the system configuration. The tubular elements are connected to control and data-readout elements by conducting lines on the substrate.

Let us consider the details of fabrication of an array of tubular elements, based on formation of thin-walled micro- and nanotubes via self-induced rolling of thin stressed heterofilms during their release from the substrate [5, 6]. It is known that the diameter of semiconductor and hybrid tubes can be accurately predetermined in the

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[1] Institute of Semiconductor Physics, Siberian Division, Russian Academy of Sciences, Novosibirsk 630090; seleznev@isp.nsc.ru; prinz@isp.nsc.ru. [2] Khristianovich Institute of Theoretical and Applied Mechanics, Siberian Division, Russian Academy of Sciences, Novosibirsk 630090; aniskin@itam.nsc.ru; maslov@itam.nsc.ru. Translated from Prikladnaya Mekhanika i Tekhnicheskaya Fizika, Vol. 50, No. 2, pp. 145–151, March–April, 2009. Original article submitted October 25, 2007; revision submitted December 24, 2007.

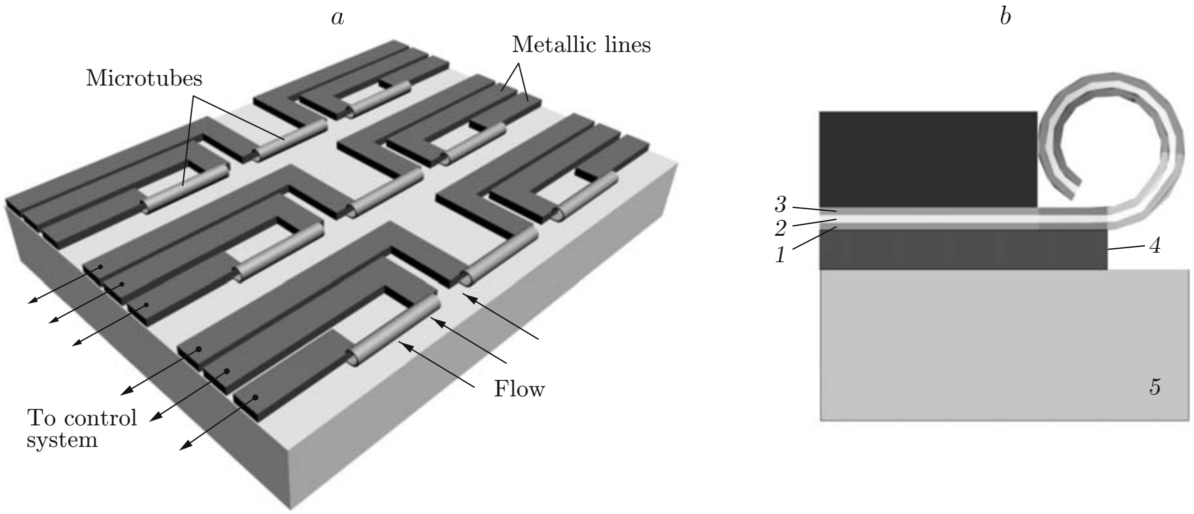

Fig. 1. System of electroconducting thin-walled microtubes with electrical contacts: (a) chip with an array of microtubes; (b) cross-sectional view of the microtube; 1) compressed layer; 2) stretched layer; 3) conducting layer; 4) sacrificial layer; 5) substrate.

range from 100 μm to 2 nm [5, 6]. Micro- and nanotubes can be formed from a wide range of materials [5–11] and can be placed at an arbitrary prescribed area on the substrate with the use of lithography. The formation of a rolled tube from a stressed multilayer film is schematically illustrated in Fig. 1b. The tube consists of compressed, stretched, and conducting layers. The compressed and stretched layers are shape-generating; they ensure rolling of the conducting layer applied onto these layers after selective removal of the substrate or an additional sacrificial layer. The compressed, stretched, and conducting layers can be fabricated from various combinations of amorphous, polycrystalline, or monocrystalline metals, dielectrics, or semiconductors [6–11].

Prototype arrays of tubular microsensors and microactuators from hybrid (metal–semiconductor and metal–dielectric) films were fabricated in a single cycle, based on the planar technology.

The most cost-effective technology is the formation of microtubes from metal layers deposited onto a silicon substrate. Plasticity and insufficient strength of amorphous metal layers, for instance, Ti/Au bi-layers, however, did not allow us to keep to this variant only. Other variants tested involved rigid shape-forming layers with sputtering of additional conducting Ti/Au metal layers.

It should be noted that the possibility of batch production of structural elements from this or that material is determined by a number of requirements, primarily, by compatibility of technological processes with standard procedures and by the possibility of fabricating free sensors and heaters protruding outside the substrate. The second requirements is satisfied if a selective etchant is available, which allows the substrate under the sensor or heater to be removed, thus, ensuring its unconstrained interaction with the gas flow.

The epitaxial InGaAs/GaAs heterofilm was chosen as a semiconductor structure. The experiments performed showed that the degree of adhesion of the deposited Ti/Au films to the semiconductor is sufficient for the formation of microtubes and removal of sacrificial layers in aqueous solutions of hydrofluoric acid.

The use of silicon substrates for tube fabrication is rather promising because of their low cost and availability of technologies for fabrication of integrated circuits. Standard technological operations for fabrication of integrated circuits are thermal oxidation of silicon and deposition of low-temperature plasmochemical silicon nitride. Young's modulus of these substances is higher than that for evaporated metals by a factor of several tens; in addition, silicon oxide obtained by thermal oxidation is in a compressed state, whereas low-temperature plasmochemical silicon nitride, vice versa, is in tension [12]. Obviously, if a stressed two-layer SiO_2/Si_3N_4 film is formed on the silicon substrate, it becomes rolled up into a tube after selective removal of the substrate. It was found that a possible selective etchant for this system can be an etchant based on aqueous solutions of ammonia [8]. For instance, two-coil tubes 5 μm in diameter were formed from a 40-nm SiO_2/Si_3N_4 heterofilm by etching the substrate for 12 h.

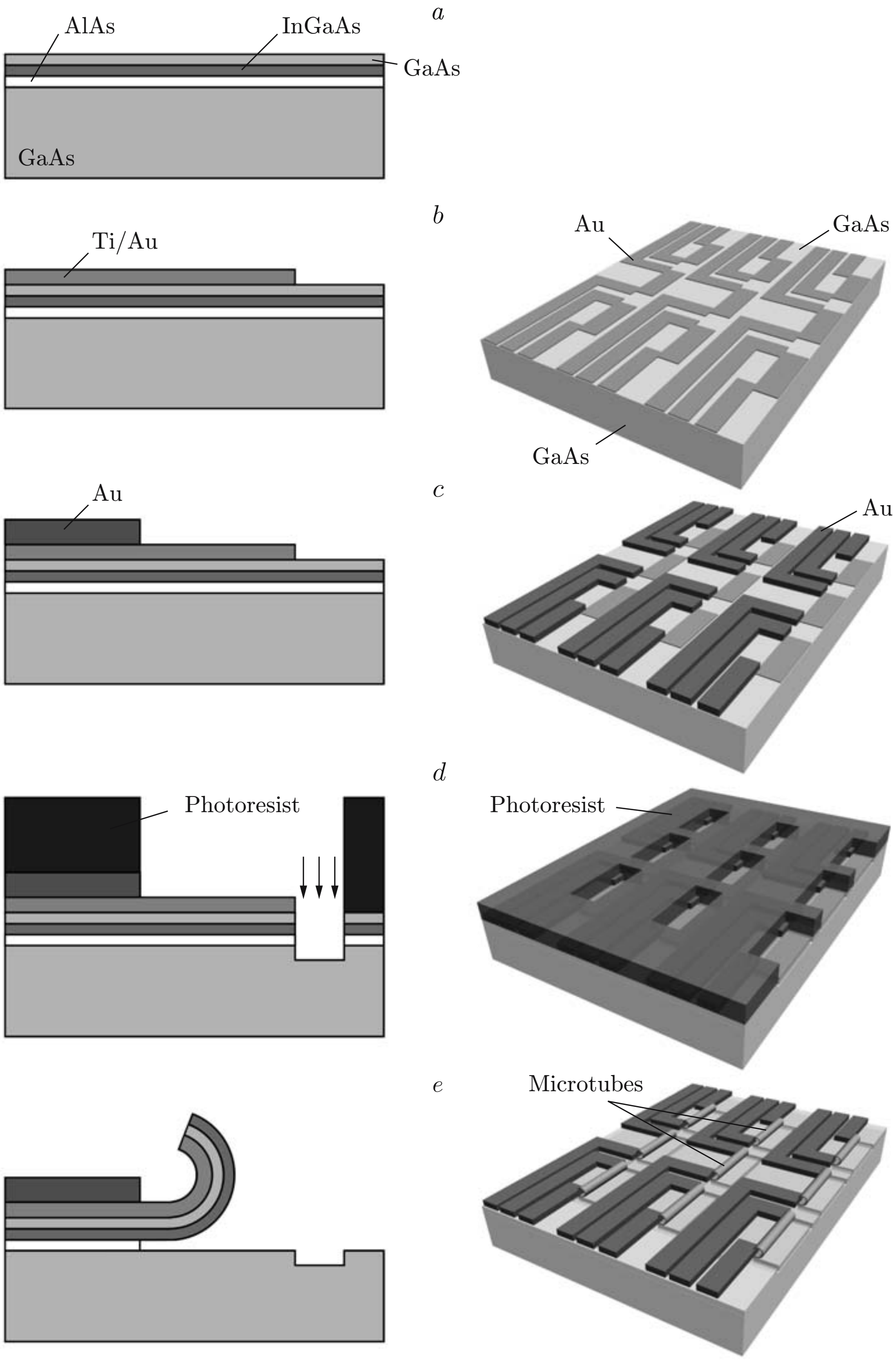

Fig. 2. Fabrication of chips with arrays of conducting microtubes based on a GaAs/AlAs/InGaAs/GaAs heterostructure: cross-sectional view (left) and general view (right); (a) formation of the AlAs/InGaAs/GaAs heterofilm on the GaAs substrate; (b) deposition of a Ti/Au layer 50 nm thick; (c) deposition of an Au layer 300 nm thick and formation of low-resistance lines; (d) etching of windows in the InGaAs/GaAs heterofilm; (e) selective etching of the AlAs sacrificial layer in the aqueous solution of hydrofluoric acid and rolling of the tube.

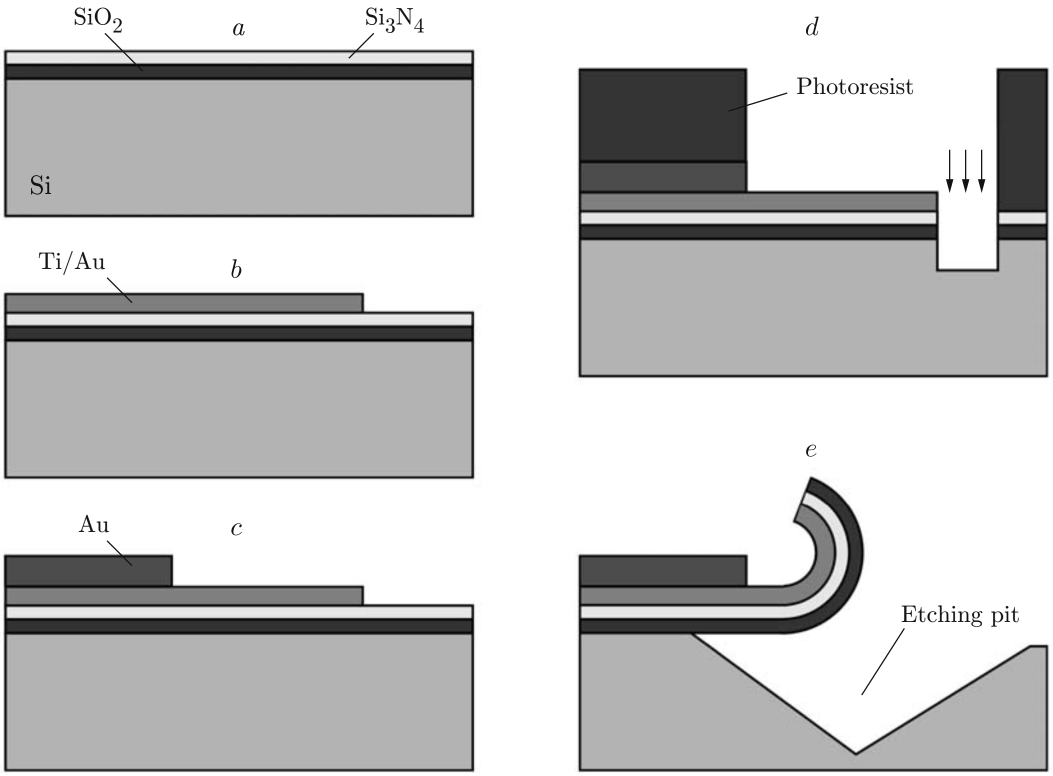

Fig. 3. Fabrication of chips with arrays of conducting microtubes based on a $Si/SiO_2/Si_3N_4$ heterostructure: (a) formation of the SiO_2/Si_3N_4 heterofilm 40 nm thick; (b) deposition of a Ti/Au layer 50 nm thick; (c) deposition of an Au layer 300 nm thick and formation of low-resistance lines; (d) etching of windows in the SiO_2/Si_3N_4 heterofilm; (e) selective etching of the substrate in the aqueous solution of ammonia and rolling of the tube.

Experiments with deposition of Ti/Au onto $Si/SiO_2/Si_3N_4$ heterostructures showed that mechanical stresses arising in the SiO_2/Si_3N_4 film being freed from the substrate are sufficient for forming tubes with an additional metal layer 50–100 nm thick.

Thus, InGaAs/GaAs and SiO_2/Si_3N_4 films were chosen as shape-forming layers in fabricating microtube arrays. The Ti/Au film was used as a conducting layer; this film was additionally deposited onto the InGaAs/GaAs and SiO_2/Si_3N_4 films by means of electron-beam evaporation (before the roll-up process).

Figure 2 shows the sequence of fabrication steps for arrays of tubular elements to be prepared from a GaAs/AlAs/InGaAs/GaAs heterostructure grown by the method of molecular beam epitaxy. A typical heterostructure contains the following layers: AlAs sacrificial layer 10 nm thick, compressed $In_{0.2}Ga_{0.8}As$ layer 16 nm thick, and stretched GaAs layer 16 nm thick (Fig. 2a). A conducting layer of a necessary planar geometry is formed on the surface of the grown heterostructure by lift-off photolithography, which involves deposition of a Ti/Au layer 50 nm thick (Fig. 2b). After that, by additional deposition of a gold layer 300 nm thick, low-resistance conducting lines are formed to regions that are microtube blanks (Fig. 2c). Then, local regions where the tubes will be formed are defined; these regions are windows in the photoresist masking layer (Fig. 2d). Plasmochemical or liquid etching of the heterofilm and, partly, of the substrate is performed through these windows, and windows in the heterofilm proper are formed (Fig. 2d). Finally, the photoresist is removed by acetone, and selective etching of the AlAs sacrificial layer by a selective etchant based on the hydrofluoric acid solution is performed [7], which results in the formation of hybrid microtubes from the InGaAs/GaAs/Ti/Au heterofilm (Fig. 2e). After that, the chips are carefully rinsed in de-ionized water and dried.

The process of fabrication of chips from $Si/SiO_2/Si_3N_4$ heterostructures (Fig. 3) is similar to the case described above.

Using the developed technological processes, we fabricated chips with arrays of hybrid microtubes rolled from $SiO_2/Si_3N_4/Au$ and InGaAs/GaAs/Au heterofilms (Fig. 4). The total thickness of the microtube walls was 90 nm

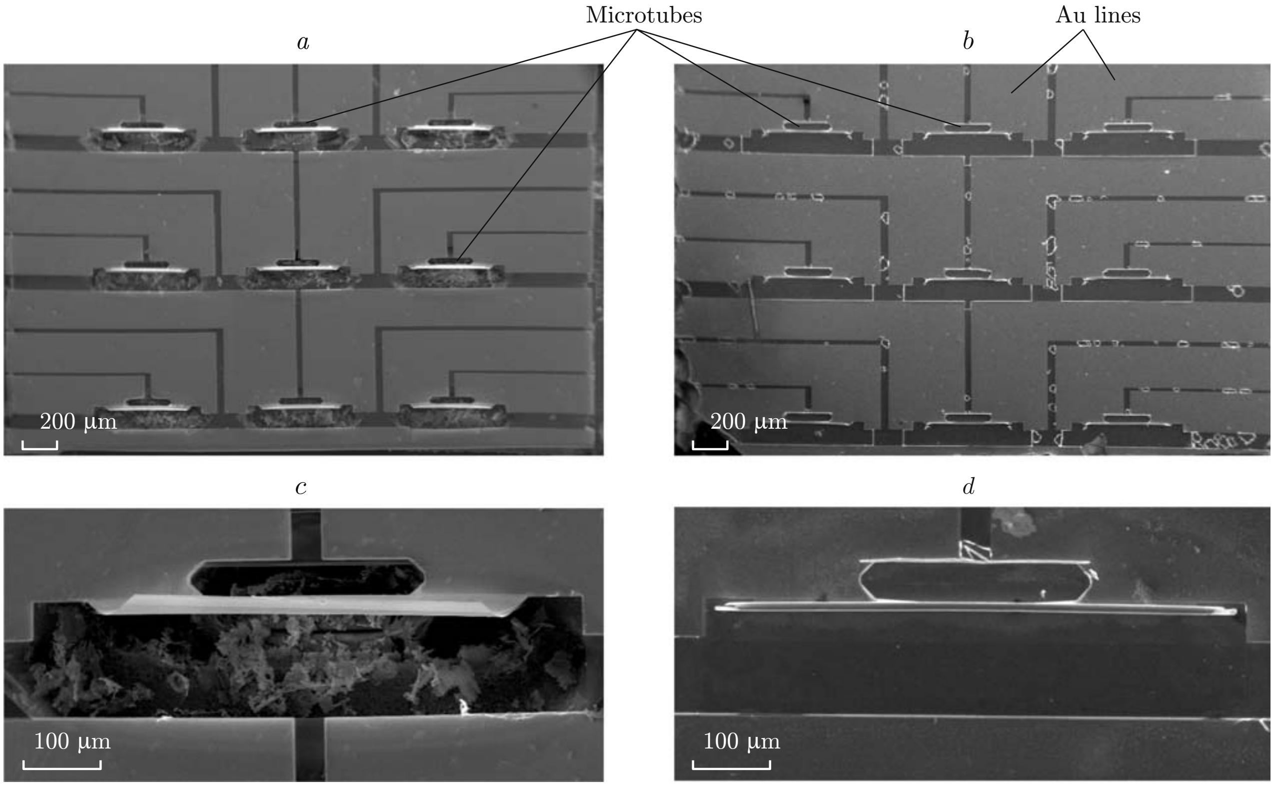

Fig. 4. Electron-microscope images of chips with arrays of conducting microtubes: (a) arrays of microtubes fabricated from the $SiO_2/Si_3N_4/Au$ heterofilm (the tubes are suspended above the pits etched in the Si substrate); (b) arrays of microtubes rolled from the InGaAs/GaAs/Au heterofilm (there are no etching pits); (c and d) zoom-in images of microtubes corresponding to Figs. 4a and 4b, respectively.

($SiO_2/Si_3N_4/Au$) and 82 nm (InGaAs/GaAs/Au). The diameter of the fabricated microtubes was approximately 10 μm. It is seen in Fig. 4a that the $SiO_2/Si_3N_4/Au$ microtubes are suspended over the pit etched in the substrate. When the GaAs/AlAs/InGaAs/GaAs/Au heterostructure is used, the tubes are suspended above the GaAs substrate at a height equal to the thickness of the AlAs sacrificial layer (see Fig. 2e). The thickness of the sacrificial layer can be defined with high accuracy (from several tens of nanometers to several micrometers). The chips fabricated on GaAs substrates have a smoother surface, which seems to be preferable in conducting aerodynamic experiments.

The methods developed allow more than 400 chips to be fabricated in one technological cycle. The number of chips is limited by the diameter of available substrates (the diameter is 76 mm for Si and 50 mm for GaAs).

Note that the semiconductor or dielectric layers of the fabricated tube are located on the outer surface, while the tube is heated by passing electric current through the gold film. The latter is extremely important for obtaining stable characteristics of tube operation (contamination of the surface by particles present in the flow changes the sensor characteristics). In the case considered, the protective coating of the metal surface by a semiconductor or a dielectric layer is formed automatically.

A significant advantage of the developed technology of fabrication of chips with distributed arrays of hybrid microtubes rolled from $SiO_2/Si_3N_4/Au$ and InGaAs/GaAs/Au heterofilms is the possibility of their batch production in a single technological process, which reduces their net cost by a factor of several tens and even hundreds.

Thus, a new approach is proposed to creating "smart" surfaces for suppressing turbulence and retaining the laminar regime of a supersonic flow. The elements of such a surface are hybrid thin-walled microtubes with electrical contacts, which can serve both as sensors and as actuators. A technology is developed for fabrication of chips with distributed arrays of microtubes, which is based on methods of self-rolling of thin stressed heterofilms into tubes and on methods used in the technology of fabrication of integral circuits. Chips with arrays of microtubes rolled from $SiO_2/Si_3N_4/Au$ and InGaAs/GaAs/Au heterofilms are fabricated.

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